

**PROCESS FOR PREPARATION OF  
SEMICONDUCTOR WAFER SURFACE**

**FIELD OF THE INVENTION**

[0001] This invention relates to semiconductor substrates and more specifically to the treatment of semiconductor substrates.

**BACKGROUND OF THE INVENTION**

[0002] Semiconductor devices such as transistors, diodes, thyristors, integrated circuits and the like are commonly made by the simultaneous processing of many identical discrete devices or integrated circuits in a common wafer.

[0003] A conventional wafer typically includes a semiconductive substrate. The substrate of a conventional wafer has a relatively high concentration of dopants (N or P), and correspondingly low resistivity. The surface resistivity across the top surface of such conventional substrates, however, is variable due in large part to the process used in the making of the ingots from which the substrates are obtained.

[0004] Semiconductor devices are typically formed on the top surface of a wafer. Generally, it is desirable to have uniform resistivity over the top surface of the wafer so that the devices formed in the wafer will exhibit substantially similar behavior. Typically, a layer of semiconductive material is epitaxially grown atop a surface of a substrate to obtain a semiconductive layer with uniform resistivity. The layer formed by epitaxial growth is conventionally referred to as an epitaxial layer or an epi layer. Epitaxial growth allows for better control of dopant concentration along the thickness of the epi layer, and thus better control over the resistivity of the epi layer.

[0005] There are substantial costs associated with epitaxial growth which increase the cost of the semiconductor devices.

[0006] It would, therefore, be desirable to eliminate the epi layer and still obtain a wafer that exhibits uniform resistivity on a top surface thereof in order to reduce the cost of semiconductor devices.

#### BRIEF DESCRIPTION OF THE INVENTION

[0007] In accordance with the invention, the resistivity across the upper surface of a conventional substrate is mapped by a suitable non-contact resistivity measuring technique. The resistivity map is then used to obtain a substantially uniform resistivity profile across the top surface of the substrate. Specifically, the resistivity of the substrate is locally adjusted (area by area) based on the resistivity map by counter-doping to obtain a uniform resistivity across the top surface of the substrate. The counter-doping can be carried out by an implanter which is controlled to counter-dope each selected area to a given target net concentration or resistivity to have a desired uniform resistivity over the full surface of the substrate. The implanted dopants are then diffused into the wafer surface for a desired depth.

[0008] In a preferred embodiment, a major surface of a conventional silicon substrate having an  $N^{++}$  resistivity of about 3 milliohm centimeters is selectively counter-doped over its full area by a controlled boron implant which, when diffused to its final depth (of about 2 to 3 microns), will have a net  $N^-$  surface resistivity of about 0.5 ohm cm. According to the present invention, the implant dose will vary over the surface of the substrate so that the final resistivity after the implant is substantially uniform over the major surface of the substrate.

[0009] According to another aspect of the invention, the resistivity of the substrate can be lowered in the ingot (from which the substrate is obtained) to, for

example, about 10 milliohm centimeters so that less counter doping is needed to adjust the surface resistivity to a substantially uniform value.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a plan view of a typical wafer according to the prior art.

[0011] Figure 2 is a cross-section of Figure 1 taken across section line 2-2 in Figure 1 viewed in the direction of the arrows.

[0012] Figure 3a is a top view of a substrate that is modified according to the present invention.

[0013] Figure 3b shows the variation of surface resistivity at the surface and across a major diameter of the substrate of Figure 3a.

[0014] Figure 4 is a flow chart of one embodiment of a process according to the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

[0015] Referring first to Figures 1 and 2, wafer 10 according to prior art consists of a substrate 11 and an N<sup>-</sup> epitaxially deposited layer (epi layer) 12. Substrate 11 is typically a monocrystalline silicon body sliced from a float zone type ingot. In a typical wafer, epi layer 12 may have a thickness of 5 to 15 microns while substrate 11 may be about 375 microns thick. Wafer 10 has bottom surface 14 and top surface 15. Substrate 11 of wafer 10 may be of the highly conductive N<sup>++</sup> (or P<sup>++</sup>) type having a low resistivity value of 3 milliohm centimeters. Epi layer 12, which receives junctions and device contacts typically has a much higher resistivity, for example, 0.5 ohm centimeters, the specific value depending on the desired breakdown voltage of the device.

[0016] Epi layer 12 has a constant resistivity across its width. In contrast, the resistivity of a major surface of substrate 11 varies as generally shown, for example, by Figure 3b. The dotted line in Figure 3b schematically shows the desired constant surface resistivity on an exaggerated scale.

[0017] In accordance with the invention, epi layer 12 is not formed on upper surface 16 of substrate 11. Rather, upper surface 16 of substrate 11 is selectively counter-doped to obtain a substantially uniform resistivity. Referring to Figure 3a, in accordance with the present invention, upper surface 16 is mapped by sampling the surface resistivity of substrate 11 at a plurality of preselected, spaced test locations, each shown, for example, by an "X" in Figure 3a. The resistivity is preferably determined by a non-contact probe using surface change profiler (SCP) technique to avoid damage to the silicon surface during mapping. For example, a suitable non-contact probe may be Epimet model 2DC provided by Semitest or QSC Series from QC Solutions.

[0018] Referring to Figure 4, according to a preferred embodiment of the present invention, the resistivity of top surface 16 of substrate 11 is adjusted to attain a substantially uniform resistivity by a software which is executed by a general purpose computer. The general purpose computer as programmed by a software to execute a method according to the present invention is schematically shown by special purpose computer 36. Referring to Figure 4, computer 36 as programmed according to the present invention first actuates a non-contact probe 20 for measuring the resistivity of a preselected area (e.g. an area marked by an X as shown in Figure 3a) in a predetermined grid on a top surface 16 of substrate 11 (see Figure 3a). Next, the resistivity of the preselected area is measured and compared 42 to a reference value. Based on the comparison of the resistivity value of the preselected area and the reference value computer 36 determines the amount of doping which may be required to counter-dope the selected area on the top surface 16 of substrate 11. The

location of the selected area and its respective counter-doping requirement are then stored in storage facility 32. The process described above is then repeated in as many selected locations on top surface 16 of substrate 11 as needed to obtain a resistivity map and proper counter-doping requirements to obtain a substantially uniform resistivity on top surface 16 of substrate 11.

[0019] The data stored in storage facility 32 are then used to counter-dope top surface 16 of substrate 11 by ion implantation unit 38. Any suitable implant species can be used for selective counter-doping. Ion implantation unit 38 implants particular locations by scanning the implant beam, or by moving the wafer under a fixed location beam with the required dose being changed from point to point to change the resistivity. Once implantation is concluded, the implants are diffused to a desired depth in a diffusion step.

[0020] As an example of the above-disclosed method and apparatus, a 3 milliohm  $\text{cm}^{-3}$   $\text{N}^{++}$  substrate can be counter-doped by a controlled boron implant beam to 0.5 ohm cm (depending on voltage rating) over its full surface and diffused to any desired depth, for example, 2 microns, or any other depth.

[0021] In accordance with a further aspect of the invention, the resistivity of the ingot, from which a substrate is obtained, can be increased during its manufacture to, for example, 10 milliohm cm. As a result, less counter-doping may be required when the resistivity of top surface 16 of substrate 11 is adjusted according to the present invention.

[0022] In the foregoing application, the invention has been described with reference to specific embodiments thereof. It, will, however be evident that various modifications and changes may be made thereto without departing from the scope of the invention as defined in the following claims.